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P R O G R A M M E

	Tutorials, Monday June 15th		
	Red Room		Green Room
9.00	Changing Role of Packaging from Packaging of ICs to Packaging of Systems with High Impact Rao Tummala Georgia Tech	9.00	Wirebonding Technologies Seminar H&K, ESEC, K&S ASM, F K Delvotec, Palomar

19.00

Welcome Cocktail

	Tuesday, June 16 th				
	Plenary Session - Main Room				
9.00	Conference Opening and	Welcome			
9.10	Keynote <i>Overview of Pack</i> <i>J.C. Eloy</i> , Yole	kaging Technologies and Ma	arkets		
9.50	Keynote <i>Automotive Pack</i> <i>B. Hauser</i> , Bosch	age Reliability			
10.30	Po	ster session and Coffee Brea	k in the Exhibition Area		
	Session 1 Blue Room	Session 2 Green Room	Session 3 Red Room	Session 4 White Room	
11.20	Evolution of Current Packaging Technologies: Flip Chip packaging	Materials: Solder Joint Properties and reliability I	Optoelectronic Packaging		
13.00		Lunch			
14.00	Evolution of Current Packaging Technologies: Embedded, Pop/Sip packages	Reliability I	Microfluidic, Medical Device Packaging		
15.40		Coffee Break in the E	XHIBITION AREA		
16.00	Evolution of Current Packaging Technologies Small form Factor	Reliability II	Ceramic Packages Including LTCC	Assembly Technology I: Wirebonding I	
	GALA DINNER				

OVERVIEW

	Wednesday, June 17 th					
	Plenary Session - Main Room					
9.00	Keynote <i>Power Packaging</i> <i>N. Abbate,</i> STMicroelectro	y onics				
9.40	Keynote <i>Package Beyond</i> <i>R. Tummala,</i> Georgia Tech	3D ICs to 3D Systems				
10.20	Po	ster Session and Coffee Brea	k in the Exhibition Area			
	Session 1 Blue Room	Session 2 Green Room	Session 3 Red Room	Session 4 White Room		
11.20	Advanced Packaging: wafer level Package I	High Power Packaging Technology	Electrical simulation			
13.00		Lunch				
14.00	Advanced Packaging: wafer level Package II	High Power Packaging: Thermal modeling and Management	Sensor Packaging	Materials: Adhesives Properties and reliability I		
15.40		Coffee Break in the E	xhibition Area			
16.00	Advanced Packaging: 3D packaging I	Materials: Solder Joint Properties and reliability II	Assembly Technology II	Substrates and Interconnects		

	Thursday, June 18th				
	Plenary Session - Main Room				
9.00	Keynote <i>Mems The future man machine interface</i> <i>B. Vigna,</i> STMicroelectronics				
9.40	 Keynote Heterogeneous Integration for System in Package H. Reichl, Fraunhofer IZM 				
10.20		Coffee Bre	AK		
	Session 1 Blue Room	Session 2 Green Room	Session 3 Red Room	Session 4 White Room	
11.20	Advanced Packaging: 3D packaging II	Mems System Packaging	Materials: Adhesives Properties and Reliability II	IMAPS Global Business Council Photovoltaics	
		Plenary Session -	Main Room		
12.30	0 Technology Knowledge Gaps Projects arising from the iNEMI Technology Roadmap B. Pfahl, J. Arnold and G. O'Malley, INEMI				
12.50	Economic Recovery Through Technological Innovation and Creativity <i>Chuck Bauer</i>				
13.10	Conference Close and pre	eview ESTC2010 and EMPC	2011		





- 1 Blue Room
- 2 Red Room
- 3 Green Room
- 4 Winter Garden

FIRST FLOOR



P R O G R A M M E

	TUESDAY, JUNE 16 [™]
	Plenary Session - Main Room Chairs: R. May - C. Cognetti
9.00	Conference Opening and Welcome
9.10	Overview of Packaging Technologies and Markets KeyNOTE SPEECH: J.C. Eloy, Yole
9.50	Automotive Package Reliability KeyNOTE SPEECH: B. Hauser, Bosch
10.30	Poster Session and Coffee Break
	Session 1 - Blue Room Evolution of Current Packaging Technologies: Flip Chip packaging Chairs: C. Cognetti - S. Noerlyng
11.20	Advancements In Bumping Technologies for Flip Chip and WIcsp Packaging D. Manessis', R. Patzelt', A. Ostmann ² , and H. Reichl ² 'Technical University Berlin, ² Fraunhofer IZM
11.45	Novel Interconnection Technique for Flip-Chip Packages; Self-Assembly Solder Bonding Technique S. Sawada, T. Kitae, S. Karashima, S. Nakatani, T. Ogawa Panasonic
12.10	New Flipchip Technology <i>R. Windemuth</i> Panasonic Industrial Europe GmbH
12.35	Characterization of oxidation of the electroplated Sn for advanced flip-chip bonding W. Zhang, and W. Ruythooren IMEC
	Session 2 - Green Room Materials: Solder Joint Properties and reliability I Chairs: B. Braux - P. Gordon
11.20	Reliability of 100 μm Bi- and In- Solder Balls S. Kemethmüller, R. Dohle, J. Pohlner, Th. Dünne, J. Goßler Micro Systems Engineering
11.45	Effect of microstructure design on reliability of FBGA lead-free solder joints <i>F.X. Che, J.E. Luan</i> STMicroelectronics

Investigation of Compliant Interconnect for Ball Grid Array (BGA) R. Johannessen, F. Oldervoll, M. V. Taklo, H. Kristiansen, H. Tyldum, HVu Nguyen, K. Aasmundtveit SINTEF ICT, Conpart AS, Norwegian University of Sciences and Technology (NTNU), Vestfold University College
Addressing Opportunities and Risks of Pb-Free Solder Alloy Alternatives G. Henshall (Hewlett Packard), R. Healey, R. S. Pandher (Cookson Electronics), K. Sweatman, K. Howell (Nihon Superior), R. Coyle, J. Smetana (Alcatel Lucent), T. Sack, P. Snugovsky (Celestica), S. Tisdale, F. Hua (Intel) and G. O'Malley (iNEMI)
Session 3 - Red Room Optoelectronic Packaging Chairs: G. Del Rosso - M. Shaw
Roll-To-Roll Manufacturing of Organic Photovoltaic Modules <i>M. Tuomikoski, P. Kopola, H. Jin, M. Ylikunnari, J. Hiitola-Keinänen, and J. Hast</i> VTT Technical Research Centre of Finland
Fully embedded optical and electrical interconnections in flexible foils <i>E. Bosman, G. Van Steenberge, P. Geerinck, J. Vanfleteren and P. Van Daele</i> Ghent University
Process Development for a Very Precise Placement of a Lens for Micro-Optics Based Components D. Caccioli, L. Maggi PGT Photonics
Packaging of silicon photonics devices: grating structures for high efficiency coupling and a solution for standard <i>J. Vicente Galan, A. Griol, J. Hurtado, J. Marti', G.B. Preve, P. Sanchis</i> NTC Universidad Politecnica Valencia
Lunch
Session 1 - Blue Room Evolution of Current Packaging Technologies: Embedded, Pop/Sip packages Chairs: P. Savolainen - J.C. Rames
Joint project for mechanical qualification of next generation high density package-on-package (PoP) with through mold via technology D. Campos, E. Saugier, M. Dreiza, J. Seong Kim, L. Smith, P. Jarvinen ST Microelectronics, Amkor Technology, Nokia
A Study of Thermal Performance for Chip-in-Substrate Package on Package <i>TYu Hung</i> ¹ , <i>MChih Yew</i> ¹ , <i>CYen Chou</i> ¹ and <i>KNing Chiang</i> ² National Tsing Hua University of Taiwan

14.50	3D integration of ultra-thin functional devices inside standard multilayer flex laminates <i>W. Christiaens, T. Torfs, W. Huwel, C.V. Hoof, J. Vanfleteren</i> CMST (Ghent University - IMEC)
15.15	Miniaturization of Printed Wiring Board Assemblies into System in a Package (SiP) S.G. Rosser, I. Memis and H. Von Hofen Endicott Interconnect Technologies
	Session 2 - Green Room Reliability I Chairs: <i>B. Hauser - N. Pat</i>
14.00	Thermo-mechanical Stress Analysis <i>K. Niehoff, T. Schreier-Alt, F. Schindler-Saefkow, H. Kittel</i> Fraunhofer IZM, Robert Bosch GmbH
14.25	In-mould Integration of Electronics into Mechanics and Reliability of Overmoulded Electronic and Optoelectronic Components <i>T. Alajoki, M. Koponen, E. Juntunen, J. Petäjä, M. Heikkinen, J. Ollila, A. Sitomaniemi,</i> <i>T. Kosonen, J. Aikio and JTapani Mäkinen</i> VTT Technical Research Centre of Finland
14.50	Assembly - Chip Interactions leading to PPM-level Failures in Microelectronic Packages A. Mavinkurve, H. Cobussen, W.D. van Driel, M. van Dort and L. Endrinal NXP Semiconductors
15.15	Creep Mechanism Fractography Analysis on Sn-Pb Eutectic Solder Joint Failure <i>C.M. Oh¹, C.W. Han¹, N.C. Park¹, S.B. Song¹, B.J. Kang², W.H. Kang² and W.S. Hong¹</i> ¹ Korea Electronic Technology Institute, ² Samsung Electronics, Republic of Korea
	Session 3 - Red Room Microfluidic/Medical Device Packaging Chairs: G. Del Rosso - P. Svasta
14.00	Advanced Microfluidic Packaging for Molecular Diagnostics <i>M. Palmieri</i> ST Microelectronics
14.25	Processes for Integration of Microfluidic Based Devices D.P. Webb, P.P. Conway, D.A. Hutt, B.J. Knauf and C. Liu Loughborough University
14.50	System packaging & integration for a swallowable capsule using a direct access sensor P. Jesudoss, A. Mathewson, B. Wright, C. McCaffrey, V. Ogurtsov, K. Twomey and F. Stam Tyndall National Institute Cork Ireland

15.15	Screen-Printed Polymer-Based Microfluidic And Micromechanical Devices Based On Evaporable Compounds N. Serra ¹ , T. Maeder, C. Jacq, Y. Fournier, P. Ryser Ecole Polytechnique Fédérale de Lausanne
15.40	Coffee Break in the Exhibition Area
	Session 1 - Blue Room Evolution of Current Packaging Technologies Small form Factor Chairs: C. Cognetti - A. Gandelli
16.00	Trends in IC Packaging C. Beelen-Hendrikx NXP Semiconductors
16.25	Realisation of embedded-chip QFP packages Technological challenges and
	A.Ostmann ¹ , D. Manessis ² , L. Boettcher ¹ , S. Karaszkiewicz ¹ , and H. Reichl ² ¹ Fraunhofer Institute for Reliability and Microintegration (IZM), ² Technical University of Berlin
16.50	WPLGA: new package family for medium pin count with design flexibility P. Magni, G. Graziosi, CM. Villa, R. Tiziani STMicroelectonics
17.15	DreamPak-Small Form Factor Package L.A. Lim, R. Malliah ASM Pacific Pte Ltd
17.40	Next Generation Leadless RF Packages Utilizing 1st Level Low Cost Flip Chip Interconnect Technology S. Walczyk, P. Dijkstra, N. Kramer, J. Verspeek NXP Semiconductors
	Session 2 - Green Room Reliability II Chairs: P. Collander - N. Sinnadurai
16.00	The necessity of corrosion protection for solderable pure tin deposits on IC outer leads P. Crema, J. Barthelmes ST Microelectronics, Atotech
16.25	Accelerating the Temperature Cycling Tests of FBGA Memory Components with Lead-free Solder Joints without Changing the Damage Mechanism <i>J. Reichelt, P. Gromala, S. Rzepka</i> Qimonda Dresden GmbH & Co.
16.50	Hydrolysis testing of ACF joined flip chip components with conformal coating <i>K. Kokko, H. Harjunpää, P. Heino, and M. Kellomäki</i> Tampere University of Technology

17.15	New packaging technology enabling integration of Magnetics and Semiconductors in one component Abel Pot, Dr. Horst Roehm, Rinus v.d. Berg, Dr. Tamim P. Sidiki DSM Engineering Plastics, NXP Semiconductors
17.40	X-ray nanoCT of interconnections in IC packages: Visualizing of internal 3D-Structures with Submicrometer Resolution J. Luebbehuesen, O. Brunke, H. Roth GE Sensing & Inspection Technologies GmbH
	Session 3 - Red Room Ceramic Packages Including LTCC Chairs: <i>M. Jakubowska - J. Mueller</i>
16.00	A Comprehensive Overview on Today's Ceramic Substrate Technologies F. Bechtold Via Electronic
16.25	Structuration of zero-shrinkage self-constraining LTCC using mineral sacrificial materials T. Maeder, Y. Fournier, C. Jacq and P. Ryser Ecole Polytechnique Fédérale de Lausanne (EPFL)
16.50	Robust LTCC/PZT Sensor-Actuator-Module for Aluminium Die Casting <i>M. Flössel</i> ⁽¹⁾ , <i>U. Scheithauer</i> ⁽¹⁾ , <i>S. Gebhardt</i> ⁽²⁾ , <i>A. Schönecker</i> ⁽²⁾ , <i>A. Michaelis</i> ⁽¹⁾ ⁽¹⁾ Technische Universität Dresden, ⁽²⁾ Fraunhofer Institut für Keramische Technologien und Systeme, Germany
17.15	3D Integration Technologies for Ceramic Substrates in a SHM Application <i>S. Hildebrandt, KJ. Wolter</i> Dresden University of Technology
17.40	Miniaturisation of a LTCC High-Frequency Rat-Race-Ring by using 3-dimensional integrated Passives and embedded High-K Capacitors <i>R. Perrone</i> ¹ , <i>J. Mülle</i> ¹ , <i>P. Kapitanova</i> ² , <i>D. Kholodnyak</i> ² , <i>I. Vendik</i> ² , <i>S. Humbla</i> ¹ , <i>M. Hein</i> ¹ ¹ Ilmenau University of Technology, Germany, ² Saint-Petersburg Electrotechnical University
	Session 4 - White Room Assembly Technology I: Wirebonding I Chairs: L. Calligarich - R. Dell'Acqua
16.00	Aluminum Ribbon on Power Device G. Cristaldi, G. Malgioglio, E. Scorfani ST Microelectronics
16.25	Mechanical properties and microstructure of heavy aluminum bonding wires for power applications <i>C. Dresbach</i> ¹ , <i>F. Naumann</i> ¹ , <i>M. Mittag</i> ¹ , <i>M. Petzold</i> ¹ , <i>T. Müller</i> ²) ¹ Fraunhofer Institute for Mechanics of Materials, Germany ² W. C. Heraeus

16.50 Surface-Enhanced Copper Bonding Wire for LSI and its Bond Reliability under Humid Environment

T. Uno Nippon Steel Corporation

17.15 Kirkendall voiding in Au ball bond interconnects on Al chip metallization at elevated temperatures from 100 - 200°C after optimizing intermetallic phase coverage

M. Schneider-Ramelow, St. Schmitz*, B. Schuch**, W. Grübl*** *Fraunhofer IZM, Germany, **Conti Temic microelectronic GmbH

17.40 Cu Wire Bonding: Reliability Improvement for High Temperature in Plastic Packages

C. Passagrilli, B. Vitali, R. Tiziani, C. Azzopardi ST Microelectronics

WEDNESDAY, JUNE 17TH

Plenary Session - Main Room Chairs: P. Collander - A. Gandelli

- 9.00 Power Packaging KEYNOTE: N. Abbate, STMicroelectronics
- 9.40 Package Beyond 3D ICs to 3D Systems KEYNOTE: *R. Tummala*, Georgia Tech
- 10.20 Poster session and Coffee Break in the Exhibition Area

Session 1 - Blue Room Advanced Packaging: wafer level Package I Chairs: C. Bauer - H. Reichl

11.20 Processing and Properties of AL-X Polymer Dielectric for Flip Chip and Wafer Level Packaging Applications

P. Garrou, A. Huffman, J. Piascik Microelectronic Consultants of NC, RTI International

11.45 Wafer Post-Processing for a Reconfigurable Wafer-Scale Circuit Board *R. Izquierdo⁽¹⁾, M. Radji⁽²⁾, O. Valorge⁽²⁾, Y. Blaquière⁽¹⁾, R. Norman, Y. Savaria⁽²⁾* Université du Québec à Montréal⁽¹⁾, École Polytechnique de Montréal⁽²⁾; McGill University Montréal, Canada

12.10	Multifunctional Coatings for Wafer-Level Chip Scale Packaging C. Brannen, R. Stapleton, P. Hough LORD Corporation, LORD Germany
12.35	Wafer Level Packaging Fan Out thermal management: is smaller always hotter? D. Gualandris, C.M. Villa STMicroelectronics
	Session 2 - Green Room High Power packaging Technology Chairs: N. Abbate - H. Osterwinter
11.20	Green high power density devices: challenges in materials science <i>A. Scandurra^a, G.F. Indelli^a, R. Zafarana^b, A. Cavallaro^b, E. Scrofani^b,</i> <i>J.P. Girib and S. Pignataro^{a.c}</i> ^a Consorzio Catania Ricerche, c/o STMicroelectronics, Catania, ^b STMicroelectronics, ^c Dip. Scienze Chimiche Università di Catania
11.45	Small Size LTCC FlipChip-Package for RF-Power Applications J. Müller ¹ , M. Noren ² , M. Mach ¹ , S. Brunner ² , C. Hoffmann ² ¹ TU Ilmenau, Germany, ² EPCOS OHG
12.10	Development of Matrix Clip Assembly for Power MOSFET packages <i>M. Kengen¹</i> , <i>W. Peels¹</i> , <i>D. Heyes²</i> ¹ NXP Semiconductors, the Netherlands - ² NXP Semiconductors, England
12.35	Reliability Studies on the high current power MODULES with parallel MOSFETs <i>G.H. Sarma et al K. Mehta et al.</i> Si2Microsystems Bangalore India - Si2 Microsytems SanJose USA
	Session 3 - Red Room Electrical simulation Chairs: N. Codreanu - A. Gandelli
11.20	Electrical Modeling and Analysis of the Impact of Slits on Microstrip Lines in Thin Film Polymer Layers <i>I. Ndip</i> ¹ , <i>M. Töpper</i> ¹ , <i>KF. Becker</i> ¹ , <i>M. Hirte</i> ¹ , <i>I. Eidner</i> ¹ , <i>T. Fischer</i> ¹ , <i>J. Bauer</i> ¹ , <i>W. Scheel</i> ¹ , <i>S. Guttowski</i> ¹ , <i>H.Reichl</i> ^{1, 2} 'Fraunhofer Institute IZM, ² Technische Universität Berlin
11.45	Impact of Package Parasitics on the EMC Performance of Smart Power SoCs <i>M. Merlin[†]</i> , <i>F. Fiori[‡]</i> [†] Istituto Superiore M. Boella, Torino, Politecnico di Torino
12.10	Advanced Modeling Techniques for System-level Power Integrity Analysis G. Graziosi [†] , P.J. Doriol [†] , Y. Villavicencio [†] , C. Forzan [†] , M. Rotigni [†] , and D. Pandini [†] [†] STMicroelectronics, [†] Politecnico di Torino

12.35	Modelling of electrostatic coupling in 3D-IC architecture <i>M. Rousseau^{1,3,4}, O. Rozeau², G. Le Carval², MA. Jaud², P. Leduc²</i> 'STMicroelectronics, ² CEA-LETI/MINATEC, ³ CNRS LAAS France, ⁴ Université de Toulouse
13.00	LUNCH
	Session 1 - Blue Room Advanced Packaging: wafer level Package II Chairs: P. Garrou - H. Reichl
14.00	Reliability comparison of Aluminum Redistribution based WLCSP Designs <i>U. Sharma, P. Holland, and H. Gee</i> California Micro Devices
14.25	The Third Dimension of eWLB <i>T. Meyer</i> ¹ <i>, A. Bahr</i> ² <i>, G. Ofner</i> ¹ <i>, R. Fürst</i> ³ <i>, X. Baraton</i> ⁴ <i>, Y. Seung Wook</i> ⁵ / ¹ Infineon Technologies Regensburg, Germany - ² Infineon Technologies Singapore ³ Infineon Technologies Neubiberg, Germany - ⁴ STMicroelectronics, Singapore ⁵ STATS ChipPAC, Singapore
14.25	Thin Hermetic Borosilicate Glass Layers for Highly Reliable Chip-Passivations in Wafer-Level-Packaging <i>U. Hansen, J. Leib, S. Maus, O. Gyenge, M. Töpper</i> MSG Lithoglas, Fraunhofer IZM
15.15	Encapsulation Challenges for Wafer Level Packaging E. Kuah, H.J. Yuan (PhD), L.Q. Fang, D.J. Pei (PhD), C.W. Ling, & SC Ho ASM Technology Singapore Pte Ltd Encapsulation Solution Group (ESG)
	Session 2 - Green Room High Power Packaging: Thermal modeling and Management Chairs: H. Osterwinter - P. Svasta
14.00	Development of space grade power hybrid for Reaction Wheel drive electronics: Challenges and criticalities <i>K. Nutheti, P. Dass, G.R. Joshi, V. and V.S Chippalkatti</i> <i>K.S. Mani*, K.P. Lilly*, M. Suresh*, T.R. Haridas* and Robert Devasahayam*</i> Centum Electronics Limited, *ISRO Inertial systems unit
14.25	 Passive Phase Change Tower Heat Sink & Pumped Coolant Technologies for Next Generation CPU Module Thermal Designs M. Vogel, D. Copeland, A. Masto, S. Kang, B. Whitney, G. Upadhya, M. Connors, J. Marsala Sun Microsystems - Aavid Thermalloy - Cooligy - Thermacore - Thermal Form and Function
14.50	A new methodology for multi-level thermal characterization of complex electronic systems : from die to board level O. Martins ¹ , N. Peltier ² , S. Guedon ² , S. Kaiser ² , Y. Marechal ¹ , Y. Avenas ¹ ¹ G2ELAB, INPG-UJF-CNRS, France - ² DOCEA Power, France

15.15	<i>M. Mach, Dr. J. Müller</i> BMBF Center for Innovation Competence MacroNano [®] , TU Ilmenau
	Session 3 - Red Room Sensor Packaging Chairs: D. Belavic - V. Sedlakova
14.00	Low energy consumption thick-film pressure sensors D. Belavic ¹ , M.S. Zarnik ¹ , M. Mozek ⁴ , S. Kocjan ³ , M. Hrovat ² , J. Holc ² , M. Jerlah ³ , S. Macek ² ¹ HIPOT-RR, Slovenia - ² Jozef Stefan Institute, Slovenia - ³ HYB, Slovenia - ⁴ Faculty of Electrical Engineering, Slovenia
14.25	The Design and Improvement of LTCC-based Capacitive Pressure Sensors employing Finite Element Analysis <i>C. Ionescu^a</i> , <i>P. Svasta^a</i> , <i>C. Marghescua</i> , <i>M. Santo Zarnik^b</i> , <i>D. Belavic^b</i> ^a University "Politehnica" of Bucharest, UPB-CETTI - ^b HIPOT-RR, Slovenia
14.50	Evaluation of Printed Electronics Manufacturing Line with Sensor Platform Application K. Kaija, E. Halonen, V. Pekkanen, and M. Mäntysalo Tampere University of Technology, Finland
15.15	 SMD Pressure and Flow Sensors for Industrial Compressed Air in LTCC Technology Y. Fournier, A. Barras, T. Maeder, P. Ryser Laboratoire de Production Microtechnique Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland
	Session 4 - White Room Materials: Adhesives Properties and Reliability I Chairs: <i>M. Jakubowska - P. Savolainen</i>
14.00	Temporary adhesives for wafer bonding: Deep reactive ion etching application <i>D. Belharet^{1,2}, P. Dubreulin^{1,2}, D. Colin^{1,2}, L. Mazenq^{1,2}, H. Granier^{1,2}</i> CNRS; LAAS; ² Université de Toulouse; UPS, INSA, INP, ISAE; LAAS
14.25	Experimental study of polymers as encapsulating materials for photovoltaic modules S. Sala, M. Campaniello, A. Bailini PV Laboratory, SEM S.r.I
14.50	Process Characterization of DuPont MXAdvance 140 Dry Film Photoresist for High Resolution Application H. Yun and C. Balut, A. Huffman, W. Liebsch DuPont Electronic Technologies, RTI International

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15.15	Fracture Toughness Assessment of ACF Flip-chip packages under High Moisture Condition with Moire Interferometry JH. Park, KW. Jang, KW. Paik, and SB. Lee	
	Department of Mechanical Engineering KAIST, Korea	
15.40	Coffee Break in the Exhibition Area	
	Session 1 - Blue Room Advanced Packaging: 3D packaging I Chairs: E. Beyne - G. Dittmar	
16.00	3D packaging and supply chain management <i>P. Collander</i>	
16.25	3DIC products using TSV for mobile phone applications: An industrial perspective <i>Y. Guillou, AM. Dutron</i> ST-NXP Wireless	
16.50	3D Integration with AC coupling for Wafer-Level Assembly <i>M. Scandiuzzo^a, L. Perugini^a, R. Cardu^b, M. Innocenti^a, R. Canegallo^a</i> ^a STMicroelectronics, ^b University of Bologna	
17.15	Direct interconnection of chemical mechanical polishing (CMP)-Cu thin films at 150°C in ambient air <i>A. Shigetou1, and T. Suga2</i> 1National Institute for Materials Science, Japan, 2The University of Tokyo	
17.40	Introduction of a unified equipment platform for UV initiated processes in conjunction with the application of electrostratic carriers as thin wafer handling solution D. Tönnies, M. Gabriel, B. Neubert, R. Ji, R. Zoberbier, M. Zoberbier, R. Völkel, M. Töpper, T. Baumgartner, I. Gräding, R. Raschke, I. Balaj SUSS MicroTec, Fraunhofer IZM, Protec Carrier Systems	
	Session 2 - Green Room Materials: Solder Joint Properties and Reliability II Chairs: A. Fairbarn - R. May	
16.00	Mechanical behaviour of SAC-lead free solder alloys with regard to the size effect and the crystal orientation J. Villain, W. Mueller, U. Saeedi, C.W. Weippert University of Applied Sciences, Germany	
16.25	NanoBond [®] Assembly - A Rapid, Room Temperature Soldering Process G. Caswell Reactive Nano Technologies	

16.50	New developments in high performance solder products for power die assemblies <i>M. Fenner</i> Indium Corporation
17.15	Au-Sn SLID bonding: Fluxless bonding with high temperature stability, to above 350oC. <i>K. Aasmundtveit^a, K. Wang^a, N. Hoivik^a, J.M. Graff^b, A. Elfving^c</i> ^a Vestfold University College, Norway, ^b SINTEF Materials and Chemistry, clnfineon Technologies SensoNor AS
17.40	Long Term Joint Reliability of SiC Power Devices at 330 <i>F. Lang</i> ¹ , <i>S. Tanimoto</i> ^{2,3} , <i>Y. Hayashi</i> ¹ , <i>H. Ohashi</i> ¹ , <i>H. Yamaguchi</i> ¹ ¹ Institute of Advanced Industrial Science and Technology (AIST), Japan ² Research and Development Association for Future Electron Devices (FED), Japan ³ Nissan Motor Co. Ltd
	Session 3 - Red Room Assembly Technology II Chairs: A. Ciappesoni - R. Dell'Acqua
16.00	Simulation and experimental analysis of substrate overmolding T. Schreier-Alt Fraunhofer IZM
16.25	Local hardening behavior of free air balls and heat affected zones of thermosonic wire bond interconnections <i>C. Dresbach¹</i> , <i>G. Lorenz¹</i> , <i>M. Mittag¹</i> , <i>M. Petzold¹</i> , <i>T. Müller¹</i> Fraunhofer Institute for Mechanics of Materials ² W. C. Heraeus
16.50	Compression Molding solutions for various high end Package applications and cost savings for standard Package applications <i>H. Matsutani</i> Towa Corporation
17.15	Advanced Failure Analysis Methods and Microstructural Investigations of Wire Bond Contacts for Current Microelectronic System Integration R. Klengel, S. Bennemann, M. Krause, Chr. Schmidt, M. Petzold Fraunhofer Institute for Mechanics of Materials
17.40	Advanced Solutions for Ultra-thin Wafers and Packaging G. Klug Disco

	Session 4 - White Room Substrates and Interconnects Chairs: F. Bechtold - J.C. Rames
16.00	High Linearity and Broadband WiMAX Power Amplifier Design Using Board Level Integration Technology WT. Chen, KC. Chin, CH. Tsai, LC. Chang, YC. Chang, and CC. Liu Industrial Technology Research Institute (ITRI), Taiwan
16.25	Packaging and wired interconnections for insertion of miniaturized chips in smart fabrics <i>J. Brun, D. Vicard, B. Mourey</i> CEA-LETI
16.50	Novel interconnection processes for low cost PEN/PET substrates <i>J.v.d. Brand', R. Kusters'.², H. Fledderus', EJ. Rubingh', T. Podprocky³, A. Dietzel'</i> 'Holst Centre/TNO - Netherlands Organisation for Applied Scientific Research, ² TNO Science and Industry - Netherlands Organisation for Applied Scientific Research, ³ Imec
17.15	Large panel, highly flexible multilayer thin film boards <i>H. Burkard, W. Kapischke, J. Link</i> Hightec MC AG, Lenzburg, Switzerland
17.40	A new low cost, elastic and conformable electronic technology for soft and stretchable electronic devices <i>F. Bossuyt</i>

University of Ghent

THURSDAY, JUNE 18[™]

Plenary Session - Main Room Chairs: D. Bokil - G. Del Rosso

- Mems the future man machine interface 9.00 KEYNOTE: B. Vigna, STMicroelectronics
- Heterogeneous Integration for System in Package 9.40 KEYNOTE: H. Reichl, Fraunhofer IZM
- 10.20 COFFEE BREAK IN THE EXHIBITION AREA

	Session 1 - Blue Room Advanced Packaging: 3D packaging II Chairs: C. Cognetti - R. Tummala
10.40	Chip to Chip bonding using micro-Cu bumps with Sn capping layers J. S. Lee and YH. Kim Hanyang University, Korea
11.05	 3D integration process flow for set-top box application: description of technology and electrical results S. Cheramy⁽¹⁾, D. Henry⁽¹⁾, A. Astier⁽¹⁾, J. Charbonnier⁽¹⁾, P. Chausse⁽¹⁾, M. Neyret⁽¹⁾, C. Brunet-Manquat⁽¹⁾, S. Verrun⁽¹⁾, N. Sillon⁽¹⁾, L. Bonnot⁽²⁾, X. Gagnard⁽²⁾, J. Vittu⁽³⁾ ⁽¹⁾CEA Léti - MINATEC, ⁽²⁾STMicroelectronics, ⁽³⁾STMicroelectronics
11.30	Modeling and Quantification of Conventional and Coax-TSVs for RF Applications <i>I. Ndip¹, B. Curran¹, S. Guttowski¹, H. Reichl^{1,2}</i> ¹ Fraunhofer Institute IZM, ² Technische Universität Berlin
11.55	Stacking of Full Rebuilt Wafers for Sip and Abandoned Sensors / Applications C. Val, P. Couderc, N. Boulay, J.C. Souriau 3D Plus, CEA-LETI Minatec
	Session 2 - Green Room Mems System Packaging Chairs: J. Mueller - B. Vigna
10.40	A 3-D packaging concept for cost effective packaging of MEMS and ASIC on wafer level T. Baumgartner, M. Töpper, M. Klein, B. Schmid, H. Kuisma, S. Nurmi, H. Kattelus, J. Dekker, R. Schachler Fraunhofer-Institut
11.05	Encapsulation of the Next Generation advanced Mems& Sensor Microsystems <i>T. van Weelden</i> Boschman Technologies B.V.
11.30	 BCB-based wafer-level packaging of integrated CMOS/SOI piezoresistive accelerometer D. Weiland*, A. Chaehoi*, D. O'Connell*, M. Begbie*, C. Wang**, S. Ray*** *Institute for System Level Integration, Livingston, **Heriot Watt University, Edinburgh, ***Semefab Ltd
11.55	Versatile MEMS and MEMS integration technology platforms for cost effective MEMS development <i>P. Pieters</i> IMEC

	Session 3 - Red Room	
	Materials: Adhesives Properties and reliability II Chairs: S. Noerlyng - T. Taddei	
10.40	Thermo Mechanical Characterization of Packaging Polymers <i>B. Boehme¹, K.M.B. Jansen², S. Rzepka³, K.J. Wolter¹</i> ¹ /Technische Universitât Dresden - ² /Delft University of Technology - ³ Qimonda Dresden	
11.05	Characteristics of Electrically Conductive Adhesives filled with Copper Nanoparticles with Organic Layer L.N. Ho*, H. Nishikawa*, T. Takemoto*, Y. Kashiwagi**, M. Yamamoto**, M. Nakamoto** *Osaka University, **Osaka Municipal Technical Research Institute	
11.30	Highly Conductive Adhesives via Novel Heterogeneous Structures T.D. Fornes, P.W. Hough LORD Corporation, LORD Germany GmbH	
11.55	Comparison between Die Attach Film (DAF) and Film Overover Wire (FOW) on Stack-die CSP Application C.L. Chung, C.W. Ku, H.C. Hsu and S.L. Fu I-SHOU University, Taiwan	
	Session 4 - White Room IMAPS Global Business Council Photovoltaics Chair: G. Caswell	
10.40	APOLLON: the Large Integrated European Project of FP7 on Concentrating Photovoltaic, target objectives on technology and cost <i>G. Timo</i> CESI RICERCA	
11.05	Crystalline Si Solar Cells: Markets and Technology <i>A. London</i> Heraeus	
11.30	Photovoltaic Present and Future - The Si potentialities D. Sartore Estelux S.p.a	
11.55	ТВА	

Plenary Session - Main Room

Chairs: E. Beyne - R. May

12.30 Technology Knowledge Gaps Projects arising from the iNEMI Technology Roadmap B. Pfahl, J. Arnold and G. O'Malley INEMI

- **12.50** Economic Recovery Through Technological Innovation and Creativity *C. Bauer*
- 13.10 Conference Close and preview ESTC2010 and EMPC2011



Poster Session

Chairs: G. Del Rosso - M. Sommaruga

Ceramics and Sensors

1. Integrated LTCC-glass microreactor and μTAS with thermal stabilization for biological application

P. Bembnowicz, D. Nowakowska, J. Leszek Wroclaw University of Technology, Poland

- Characterization of PTC resistor pastes applied in LTCC technology J. Vanek, W. Smetana¹, I. Szendiuch Brno University of Technology, Brno, Czech Republic - ¹Vienna University of Technology
- Influence of the Fabrication Errors on Multilayer Thick Film Circuits W. Ali¹, C. Min, N. Osman², and C. Free²
 ¹College of Technological Studies, Kuwait - ²University of Surrey
- 4. Long Term Stability of Polymer Based Resistors Tested by Noise, Non-Linearity and Electro-Ultrasonic Spectroscopy V. Sedlakova, P. Tofel, J. Sikula Brno University of Technology
- 5. Interface Resistance between Polymer Based Conducting and Resistive Layers V. Sedlakova, P. Tofel, M. Chvatal, J. Sikula Brno University of Technology
- 6. Bisected thermodynamic sensor as the power AC/DC transmitter *R. Michal*⁽¹⁾, *S. Ivan*⁽¹⁾, *R. Zdenek, Jr.*⁽²⁾, *R. Zdenek, Sr.*⁽³⁾, ⁽¹⁾Department of Microelectronics, Brno University of Technology - ⁽²⁾Department of Radio Electronics, Brno University of Technology - ⁽³⁾HIT Ltd, Czech Republic
- 7. Development of low-firing lead-free thick-film materials for piezoresistive sensors on steel substrates

C. Jacq, T. Maeder, and P. Ryser Ecole Polytechnique Fédérale de Lausanne

Materials Adhesives, Solder Properties and Reliability

8. Size and Microstructure Effects on the Stress-Strain Behaviour of Lead Free Solder Joints P. Hegde, D.C. Whalley and V.V. Silberschmidt Loughborough University, UK 9. A Study on High-density High-speed SerDes Design in Buildup Flip Chip Ball Grid Array Packages

G. Xiang, P. Brunet, K. Sheach High Speed Package Design, Ottawa Design Center, STMicroelectronics

10. Investigation of Solder Joints by Thermographical Analysis

P. Svasta^a, *C. Ionescu^a*, *N.D. Codreanu^a*, *D. Bonfert^b* ^aUniversity "Politehnica" of Bucharest - ^bPS, Fraunhofer Institute Reliability and Microintegration / IZM-M

11. Experimental Characterization Of Thermo-Mechanical Properties Of Lead-Based Solders For Power Electronics Packaging Reliability Applications

S. Jacques^{(a)(b)}, J. Roubion^(c), N. Bastut^(b), R. Leroy^(c), L. Gonthier^{(a)(b)(a)} ^(a)STMicroelectronics - ^(b)"Laboratoire de Microélectronique de Puissance (LMP)", University of Tours, France - ^(c)"Laboratoire de Mécanique et Rhéologie (LMR)", University of Tours

12. Solder Process Optimization: Influence of Heating and Cooling Rate on the Thermo-Mechanical Stress Generated in Components

M. Hertl, D. Weidmann, J.C. Lecomte INSIDIX

- Effects of test conditions on bending impact of lead free solder *J. Park* RIST - South korea
- 14. Mechanical and Microstructural Properties of SiC-Mixed Sn-Bi Solder Bump C.W. Lee, Y.S. Shin, S. Lee, S. Yoo Korea Institute of Industrial Technology
- 15. A Novel Thermo-Mechanical Method of Fatigue Characterization of Real Solder Joints

R. Metasch, M. Röllig**, K.J. Wolter* *TU-Dresden - **Fraunhofer Institut für Zerstörungsfreie Prüfverfahren

16. Pot Life Improvement of Low Temperature and High-speed Curable Anisotropic Conductive Adhesive

J.H. Lee*, J.H. Kim, C.Y. Hyun Seoul National University of Technology

- 17. Experimental analysis on the mechanism of moisture induced interface weakening in ACF package *G.D. Sim* KAIST - Korea
- 18. New Facts from Lead-free Solders Reliability Investigation

I. Szendiuch, J. Jankovsky Brno University of Technology

Reliability

- **19. Fine D.A. Delamination analysis by Acoustic Microscope** *G. Santospirito, A. Terzoli* ST Microelectronics
- 20. Metal Trace Impact Life Prediction Model for Stress-Buffer-Enhanced Package C.-Y. Chou, C.-J. Huang, M. Sano, and K.-N. Chiang National Tsing Hua University, HsinChu, Taiwan
- 21. Design and Fabrication of Corrosion and Humidity Sensors for Performance Evaluation of Chip Scale Hermetic Packages for Biomedical Implantable Devices *N. Saeidi* University College London
- **22.** Connector reliability testing using salt spray *A. Parviainen, J. Perälä, S. Kuusiluoma, and L. Frisk* Tampere University of Technology
- 23. Investigation of the Relationship between Material Selections and Moisture Sensitivity Levels of Quad Flat No-lead (QFN) Packages

M. Zhang and S.W. R. Lee Hong Kong University of Science and Technology, Clear Water Bay

- 24. Fatigue Life Prediction of Plated Through Holes(PTH) under Thermal Cycling N.-C. Park, C.-M. Oh, B.-S. Song, C.-W. Han, W.-S. Hong Korea Electronics Technology Institute
- 25. Damage Risk Assessment of Under-Pad Structures in Vertical Wafer Probe Technology

T. Hauck, I. Schmadlak*, W.H. Müller*** *Freescale Halbleiter Deutschland GmbH - **Technische Universität Berlin

26. Reliability Testing of Frequency Converters with Salt Spray and Temperature Humidity Tests

J. Kiilunen, L. Frisk Tampere University of Technology

Simulation

27. Application of 3D modeling tools for advanced packaging on a broad range of industrial applications

Y. Imbs¹, L. Marechal¹, D. Auchere¹, G. Graziosi², J. Debono³ STMicroelectronics Grenoble¹, Agrate², Kirkop³

28. Electromagnetic Simulations For The Packaging Design Of Telecommunication Component

L. Maggi, G. Ticozzi PGT PHOTONICS SpA 29. Modeling of Flip Chip Bump Patterns to minimize Crosstalk on a BU-BGA package design

P. Brunet, K. Sheach, G. Xiang High Speed Package Design, Ottawa Design Center, STMicroelectronics

- **30.** Thermoelastic Properties of Printed Circuit Boards II: Effect of Copper Trace *H. Guojun, G.K. Yong, L. Jing-en, L.W. Chin and X. Baraton* STMicroelectronics
- **31.** Far-End Maximum Crosstalk for Coupled Lines as a Function of Load A. Owzar, R. Stephan, W. Petersen, M. Helfenstein

ST-Wireless

Package Assembly and Design

- **32. Latest Plasma Cleaning Technology** *R. Windemuth* Panasonic Industrial Europe GmbH
- **33. Electrostatic wafer handling for thin wafer processing** *C. Landesberger, R. Wieland, A. Klumpp, P. Ramm, A. Drost, U. Schaber, D. Bonfert, K. Bock* Fraunhofer-Institute for Reliability and Microintegration IZM
- 34. Optimization of Flip-chip Laser Soldering for Low Temperature Stability Substrate

T. Hurtony, B. Balogh, P. Gordon Budapest University of Technology and Economics

35. Novel methodology for analyzing variation risk introduced by the manufacturing and/or assembly process in Microsystems

Y. Sun¹, *C.R Fowkes²*, *N. Gindy¹* ¹University of Nottingham, UK - ²Knowledge Transfer Network,UK

- **36. High speed packaging solutions for LiNbO3 electro-optical modulator** *S. Bonino, R. Galeotti, L. Gobbi* Avanex
- 37. Fabrication & characterization of S-band power amplifier MMIC (GaAs Die) implemented in hybrid fixture.

B. N. Shahzad National Engineering & Scientific Commission (Nescom), Islamabad

38. MEMS Pressure sensors - new LGA Packagings

L. Baldo, M. Azzopardi,** F. Fontana***, S. Gatt *** *ST MEMS & Healthcare, **ST Microelectronics Corporate Packaging and Automation ***ST Microelectronics Corporate Packaging and Automation

39. Package design for alleviating stress in materials embedded with electronic systems

M. Lishchynska, K. Delaney Cork Institute of Technology



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Tuesday, June 16th:	9.00 - 18.00
Wednesday, June 17 th :	9.00 - 18.00
Thursday, June 18th:	9.00 - 13.00

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CPS is the world leader in providing AISiC thermal management materials, designs and products for the microelectronics and power electronics industries. Applications include pin film coolers for IGBT modules in hybrid electric vehicles, motor control power modules, DC/DC converters, high voltage power factor correction, uninterruptible power supplies and many others.







microcontrol



PADAR tecnologie







BOOTH N. 14

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B00TH N. 21

33

ELECTROVAC Curamik GmbH Im Gewerbepark D 75 - 93059 Regensburg Germany Ph. 0049.941.69809033 - 0049.941.68809099 OMA@electrovac.com - www.curamik.com

Curamik electronics is the market and technology leader in Direct Bonded Copper products (DBC), such as ceramic printed circuits boards and cooling systems. Application areas include energy management for the automotive industry in hybrid vehicles, fork lifts, traction control, inverters for photo-voltaic systems, wind generators and home appliances.

Batten & Allen

Bridge End - Love Lane Trading Estate Cirencester - Gloucestershire - England GL7 1NQ Ph. 0044.1285.655220 - Fax 0044.1285.652650 dwilson@batten-allen.co.uk - www.batten-allen.co.uk

Specialised stamping and plating of strip terminals and contacts is at the heart of Batten & Allen business to create precision products. Application is for second level and intermediate level assembly in a wide variety of fields including the medical, telecom, automotive and electronic industries.

ESL Europe

8 Commercial Road - Reading - Berkshire England RG2 0QZ Ph. 0044.118.9182425 - Fax 0044.118.9867331 KJones-Williams@esleurope.co.uk - www.electroscience.com

ESL - Electro Science Labs manufacture screen-printable pastes such as thick film conductors, dielectrics and resistors, ceramic tape systems and fired parts like porous alumina and zirconia cover plates. Applications are in hybrid microcircuits, multilayer microelectronics, chip components, heaters on steel and other substrates, photovoltaic solar cells, SOFC and other fuel cells.

Panasonic Factory Solutions Europe a Division of Panasonic Industrial Europe GmbH Hans-Pinsel-Straße 2 - D-85540 Haar Tel.: + 49 (0) 89 / 46159 - 365 - Fax: 49 (0) 89 / 46159 - 260 Mobile: + 49 (0) 173 / 6 259 225

e-mail: Reinhard.Windemuth@eu.panasonic.com

Flipchip Bonding - Dieattach - Plasma Cleaning

Poltronic Ltd.

Consulting and networking in microelectronics and packaging Paul Collander Espoo, Finland paul@poltronic.fi - www.poltronic.fi

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SUSS MicroTec

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BOOTH N. 25

GENERAL INFORMATION

Secretariat Hours

Monday, June 15 th :	8.30 - 18.30
Tuesday, June 16 th :	8.30 - 18.30
Wednesday, June 17th:	8.30 - 18.30
Thursday, June 18th:	8.30 - 13.00

Speakers

All speakers are kindly requested to meet their chairperson at the speaker room (1st floor) 15 minutes before the beginning of their session All presentations must be given to the technician of the speakers room at least one hour before the beginning of the Session

Coffee Breaks and Meals

Coffee breaks will be served in the exhibition area. Lunch will be served in the restaurant on the ground floor.

Lunch tickets can be found inside the registration envelope. Additional tickets are available at the secretariat desk (\notin 28,00)

Badge

You will be requested to wear your personal badge to enter the Conference Rooms.

Social Programme

Monday June 15th, 19.00: Welcome Cocktail for all participants and exhibitors Winter Garden, 1st floor Extra tickets can be bought at the Secretariat desk (€ 28,00)

Tuesday June 16th, 20.00:

Gala Dinner at Rimini Grand Hotel Parco Federico Fellini Extra tickets can be bought at the Secretariat desk (€ 80,00)

Accompanying Persons' Programme

Tuesday June 16th: Visit of San Marino (half day)

Guided tour of San Marino to discover the most important monuments of the historical centre: the citadel, the small city centre with its districts and ancient stone buildings and the three mediaeval castles with an incomparable view that extends from the Tuscan-Romagna Appennine mountains to the Adriatic coast.

A trip, not only touristic, into the legend of a country which has been able to safeguard its thousands of years of history.

Rate per person € 25,00 inclusive of: transfer by coach, hostess, tour guide of the city (1 hour), free time for shopping. Entrance tickets to the monuments are not included. Valid for a group of minimum 30 people. For confirmation ask the secretariat

Wednesday, June 17th: Visit of Ravenna (full day)

A visit to the last capital of the Roman Empire in the West, Ravenna, that still preserves superb examples of Byzantine art: the mosaics. Eight of its religious buildings decorated with mosaics have been declared patrimony of humanity by UNESCO. You will then enjoy a delicious Italian lunch in a restaurant of the city centre and continue with a visit of Dante's Tomb and Museum. The tour ends with a stop just outside Ravenna, to see the beautifully located Basilica of Sant'Apollinare in Classe whose magnificent mosaics would alone be well worth a visit.

Rate per person € 75,00 inclusive of: transfer by coach, hostess, tour guide of the city (up to 6 hours visit), lunch, Vat. The above mentioned rate do not include the entrance tickets to the monuments. The cost of the ticket that includes the entrance to S.Vitale, Galla Placidia, Battistero Neoniano, Museo Arcivescovile, Sant' Apollinare in Nuovo, is of € 7,50 per person, to be paid directly on the spot.

The cost of the ticket for the Basilica of Sant' Apollinare in Classe is of \in 3,00 per person, to be paid directly on the spot.

The rate in valid for a group of minimum 30 people. For confirmation ask the secretariat

Tourist Information

For turistic maps and information on public transportation, please contact the APT desk in the Palacongressi main hall.



Grand Hotel di Rimini